

Appl. No. 10/707,514
Amdt. dated April 06, 2005
Reply to Office action of January 13, 2005

AMENDMENTS TO THE CLAIMS

1. (currently amended) A method for performing
non-integer frequency division, providing at least an
5 output clock according to a plurality of reference
clocks, and making the period of the output clock a
predetermined multiple of the period of the reference
clocks, the method comprising:
receiving a plurality of reference clocks, the
10 periods of the reference clocks being the same,
and the phases between the different reference
clocks being different;
triggering a plurality of intermediate signals
according to each period of the reference clocks,
15 there being M intermediate signals for each
reference clock, and making the minimum period
of the intermediate signals an integer multiple
of M times the period of the corresponding
reference clock, the phases between the
20 intermediate signals corresponding to the same
reference clock being different; and
performing a logic operation between at least two
intermediate signals respectively
corresponding to two different reference
25 clocks, providing an output clock according to
the result of the logic operation, the minimum
period of the output clock being shorter than
the period of the intermediate signals.

Appl. No. 10/707,514

Amdt. dated April 06, 2005

Reply to Office action of January 13, 2005

2. (currently amended) The method of claim 1 wherein when receiving N reference clocks each identified by an integer n ranging from one to N, the phase difference
5 between the n-th reference clock and the first reference clock is $((n-1)/N)*360$ degrees.
3. (currently amended) The method of claim ~~[[1]]~~ 2 wherein ~~the triggering step makes the minimum period of the intermediate signals M times the period of the reference clock,~~ when the period of the reference clock is T, the period of the output clock is $L*(T/N)$, L being one of the factors of $M*N$.
10
4. (currently amended) The method of claim 1 wherein ~~the triggering step triggers M intermediate signals according to each reference clock, making the minimum period of the intermediate signals M times the period of the reference clock,~~ each of M intermediate signals
15 is identified by an integer m ranging from one to M and the phase difference between the m-th intermediate signal and the first intermediate signal ~~[[being]]~~ is equal to m times the period of the reference clock.
20
5. (cancelled)
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6. (original) The method of claim 1 wherein the period of each intermediate signal kept at a first level is

Appl. No. 10/707,514
Amdt. dated April 06, 2005
Reply to Office action of January 13, 2005

an integer multiple of the period of the reference clock.

7. (currently amended) The method of claim 1 wherein when
5 performing the triggering step, [[a]] the plurality
of the intermediate signals is generated by
edge-triggering.

8. (original) The method of claim 1 wherein the period
10 of the output clock is shorter than the period of the
reference clocks.

9. (currently amended) A signal circuit for providing
at least one output clock according to a plurality of
15 reference clocks, making the period of the output clock
a predetermined multiple of the period of the reference
clocks, the signal circuit comprising:

a reference clock circuit for providing a plurality
of reference clocks, the periods of reference
20 clocks being the same, and the phases between
the different reference clocks being
different;

a triggering module including a plurality of state
machines, each state machine corresponding to
25 a reference clock, for triggering a plurality
of [[the]] corresponding intermediate signals
according to each period of the reference clocks,
there being M intermediate signals for each

Appl. No. 10/707,514
Amdt. dated April 06, 2005
Reply to Office action of January 13, 2005

5 reference clock, and for making the minimum
 period of the intermediate signals ~~an integer~~
 ~~multiple of M times~~ the period of the
 corresponding reference clock, the phases
10 between the intermediate signals corresponding
 to the same reference clock being different; and
 a logic module including a plurality of logic gates,
 the logic module performing a logic operation
 between at least two intermediate signals
15 respectively corresponding to two different
 reference clocks, providing an output clock
 according to the result of the logic operation,
 the minimum period of the output clock being
 shorter than the period of the intermediate
 signals.

10. (currently amended) The signal circuit of claim 9
 wherein the reference clock circuit provides N
 reference clocks each identified by an integer n
20 ranging from one to N, the phase difference between
 the n-th reference clock and the first reference clock
 being $((n-1)/N) * 360$ degrees.

11. (currently amended) The signal circuit of claim 10
25 wherein ~~each state machine makes the minimum period~~
 ~~of each intermediate signal M times the period of the~~
 ~~reference clock~~, when the period of the reference
 clocks is T, the period of the output clock is $L * (T/N)$,

Appl. No. 10/707,514
Amdt. dated April 06, 2005
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L being one of the factors of $M \cdot N$.

12. (currently amended) The signal circuit of claim 9
wherein ~~the state machines trigger M intermediate~~
5 ~~signals according to each reference clock, making the~~
~~minimum period of each intermediate signal M times the~~
~~period of the reference clocks, each of M intermediate~~
~~signals is identified by an integer m ranging from one~~
10 ~~to M and the phase difference between the m-th~~
~~intermediate signal and the first intermediate signal~~
~~[[being]] is equal to m times the period of the~~
~~reference clocks.~~

13. (cancelled)
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14. (original) The signal circuit of claim 9 wherein the
period of each intermediate signal kept at a first
level by each state machine is an integer multiple of
the period of the reference clock.
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15. (currently amended) The signal circuit of claim 9
wherein each state machine generates ~~[[a]]~~ the
plurality of the intermediate signals by
edge-triggering.
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16. (original) The signal circuit of claim 9 wherein the
period of the output clock generated by the logic
module is shorter than the period of the reference

Appl. No. 10/707,514
Amdt. dated April 06, 2005
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clocks.